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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,134	12/10/2003	Hsiao-Ying Yang	0941-0871P	4687

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,134	YANG, HSIAO-YING	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,7,10 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the claims

1. Claims 1, 2, 5, 7, 10 and 11 and are now pending in the application.

2. Claims 1, 2, 5, 7, 10 and 11 are treated on the merit as set forth herein below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5, 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hurley et al. (US/2002/0130357) in view of Hung et al et al. (US/5,214,305).

Re claim 1, Hurley et al. disclose a floating gate having improved coupling ratio, comprising: a semiconductor substrate (501); a tunneling dielectric layer (502) formed on the semiconductor substrate (501); a conductive layer (503), formed on the tunneling dielectric layer (502) (see Figs. 5A-5F); and a plurality of conductive spacers (509), formed on the sidewalls of the conductive layer (503) (see Fig. 5G), and the tops of the conductive spacers level with the surface of the conductive layer, with the conductive spacers and the conductive layer forming the floating gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Although Hurley et al. use a polysilicon as conductive material to form conductive spacers (509) on the conductive floating gate structure (503), Hurley et al. do not specifically disclose use of polycide to form conductive spacers and floating gates. However, such material

choice is well-known in the art and within the level of ordinary skill in the art to at the time of the invention made.

Hung et al. disclose fabricating of MOSFET for IC using a polycide gate. Hung et al. disclose that "The use of polycide gates or interconnect lines, that is a combination of layers of polysilicon and a refractory metal silicide is becoming very important as the industry moves to smaller device geometries. In the past, polysilicon was satisfactory as the gate electrodes and for interconnecting lines. However, as these geometries become smaller, polysilicon has become too high in resistivity for these applications due to its affect on RC time delays and IR voltage drops. The use of a combination of refractory metal silicides with polysilicon has proven suitable because of its lower resistivity." (see Hung et al. Col. 1, lines 16-27).

Both Hurley et al. and Hung et al. teachings are directed to method of fabricating semiconductor devices that includes forming a conductive sidewall spacers. Therefore, the teachings of Hurley et al. and Hung et al. are analogous.

Hence, one of ordinary skill in the art would have motivated to use a gate material contains polycide in order to achieve low resistive gate material. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Hurley et al. reference with polycide gate material as taught by Hung et al. because the polycide has lower resistivity than polysilicon and that would have lead to fabrication of high performance miniaturized device.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use polycide material instead of polysilicon for gate formation, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of

its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (CCPA 1960).

Re claim 2, as applied to claim 1above, Hurley et al. and Hung et al. in combination disclose all the claimed limitations including the limitation two neighboring shallow trench isolation structures (507), and the tunneling dielectric layer (502) (see Fig. 5C) located between the two shallow trench isolation structures (507) gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 5, as applied to claim 1above, Hurley et al. and Hung et al. in combination disclose all the claimed limitations including the limitation wherein the tunneling dielectric layer is oxide or oxynitride (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 7, Hurley et al. disclose a floating gate having improved coupling ratio, comprising: a semiconductor substrate (501); a tunneling dielectric layer (502) formed on the semiconductor substrate (501); a conductive layer (503), formed on the tunneling dielectric layer (502); a pair of shallow trench isolation (507) formed oppositely adjacent to the conductive layer (503), wherein the shallow trench isolation (507) is lower than the top surface of the conducting layer (503) (see Fig. 5D); and a plurality of conductive spacers (509), formed on the sidewalls of the conductive layer (503) and overlying the shallow trench isolation (507), and the tops of the conductive spacers (509) level with the surface of the conductive layer (503) (see Fig. 5G), with the conductive spacers and the conductive layer forming the floating gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Although Hurley et al. use a polysilicon as conductive material to form conductive spacers (509) on the conductive floating gate structure (503), Hurley et al. do not specifically disclose use of polycide to form conductive spacers and floating gates. However, such material choice is well-known in the art and within the level of ordinary skill in the art to at the time of the invention made.

Hung et al. disclose fabricating of MOSFET for IC using a polycide gate. Hung et al. disclose that "The use of polycide gates or interconnect lines, that is a combination of layers of polysilicon and a refractory metal silicide is becoming very important as the industry moves to smaller device geometries. In the past, polysilicon was satisfactory as the gate electrodes and for interconnecting lines. However, as these geometries become smaller, polysilicon has become too high in resistivity for these applications due to its affect on RC time delays and IR voltage drops. The use of a combination of refractory metal silicides with polysilicon has proven suitable because of its lower resistivity." (see Hung et al. Col. 1, lines 16-27).

Both Hurley et al. and Hung et al. teachings are directed to method of fabricating semiconductor devices that includes forming a conductive sidewall spacers. Therefore, the teachings of Hurley et al. and Hung et al. are analogous.

Hence, one of ordinary skill in the art would have motivated to use a gate material contains polycide in order to achieve low resistive gate material. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Hurley et al. reference with polycide gate material as taught by Hung et al. because the polycide has lower resistivity than polysilicon and that would have lead to fabrication of high performance miniaturized device.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use polycide material instead of polysilicon for gate formation, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (CCPA 1960).

Re claim 10, as applied to claim 7 above, Hurley et al. and Hung et al. in combination disclose all the claimed limitations including the limitation wherein the tunneling dielectric layer is oxide or oxynitride (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 11, as applied to claim 7 above, Hurley et al. and Hung et al. in combination disclose all the claimed limitations including the limitation wherein the shallow trench isolation is an oxide layer (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Response to Arguments

5. Applicant's arguments with respect to claims 1, 2, 5, 7, 10 and 11 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on November 9, 2004.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
January 18, 2005

George Fourson
Primary Examiner